JOURNAL OF CRITICAL REVIEWS

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

PERFORMANCE COMPARISON OF OPTIMIZED QUANTIZATION IN REAL-TIME DISTRIBUTED WIRELESS NETWORK

S.P.Manikanta[1], K.Rameshchandra[2], Dr.P.Santosh Kumar Patra[3]

[1]Associate Professor, St.Martin's Engineering College, Secunderabad-500100, India.
[2]Associate Professor, Vishnu Institute of Technology, Bhimavaram - 534202
[3]Principal & Professor in CSE, St.Martin's Engineering College, Secunderabad-500100, India.

[1]spmanikantaece@smec.ac.in, [2]rameshchandra.k@vishnu.edu.in, [3]drpskpatra@gmail.com

ABSTRACT: Digital signal processing is most important for handling all the electronic components and processes the signals. Computing devices knows only binary values. DSP is used to identify the signal, process it and covert into computer understandable format. Quantization is the process of generating error codes in distributed network and compare the result. These papers propose an optimized quantization method to reduce the quantization error and reduce the communication cost. The communication cost is the important factor to set digital system. In our proposed method, we implement novel method in real time-hardware digital system in optimized way. Real time systems are implemented using DSP hardware, FPGAs, GPUs and General purposes. We introduced windows based graphics instrument with DSP Processor. In this model has network topology and iterative method for handling signal. Our results show the proposed method has efficient performance and minimizing quantization error with low budget design.

KEY WORDS: Digital signal processing, distributed network, optimized quantization, topology, low budget design

I. INTRODUCTION

The signal processing provides many applications such as denosing, restoration, sensor computing and compression. All the signal process applications require distributed processing and well defined design. The computation is another important factory to deal signals, network data and performance. Chebyshev polynomials are used to process the signals and produce the comparison results. In this case, communication is constraint and limit precision factor. We need effective design to handle network data and signals with low budget model [1].

The various factors are affecting the digital system but mainly focus on hardware components such as DSP board, circuit design, camera, sensor and microprocessor. Nowadays the usage of computing devices and utilization is very high. For example, over the five years, smart phones, tablets, GPUs and low cost microprocessor are in the market. Small configuration and coding leads different results. IoT design and components is playing vital role in different real time applications [2].

This case, we identified very expensive and GPU process board are used for variety of applications. The investment and design cost are two important factors [3]. The platforms with professional DSP processor and development tools are used. This kind of modelling and programming are adopt changes and implementation are need in real time. In this paper divided into following sections, section II deals various related works, section 3 describes system model and descriptions, section 4 explains implementation, section 5 is conclusion and discussions.

II. RELATED WORKS

Quantized graph signal processing has linear prediction factor and provides graph based histogram results [4]. Isebela et al, the effect of quantization leads mitigating numerical effects, finite precision and filtering. This is central decision making phenomena and each hardware has specific feature. The design of digital system with finite precision and limited communication devices are the important characteristics. Another important factor is solving network error and quantized communication [5][6].

Frossard et al, the quantizer performance is evaluated by using bounded messages. The mean square error and bit allocation are major consideration. The performance can be computed using uniform quantizer and the values are uniformly distributed [7]. The error propagates to all nodes and difficult to compute distributed delays. Here, general processing tasks are computed using quantization noise.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

Wright et al, the computation of digital components can affect following reasons, 1. Purchase of own components and design, 2. The common platforms are used for all the computation. So this case availability, affordability and suitability are considered and based on that we must take effective decision [8]. The above literatures and discussions, we design a novel digital system with less quantization error. This paper focuses a fully optimized bit allocation method and effective decision making capabilities [9].

III. SYSTEM MODEL AND DESIGN

We used windows DSK with programming kit for implementing our proposed model. Set of real-time hardware components with program support are used. Here windows based floating point texas interface, real-time DSP board and software are selected. DSP kit mentioned Ti C67 OMAP model are used connected distributed networks. The following figure 1 show that hardware component and DSP board

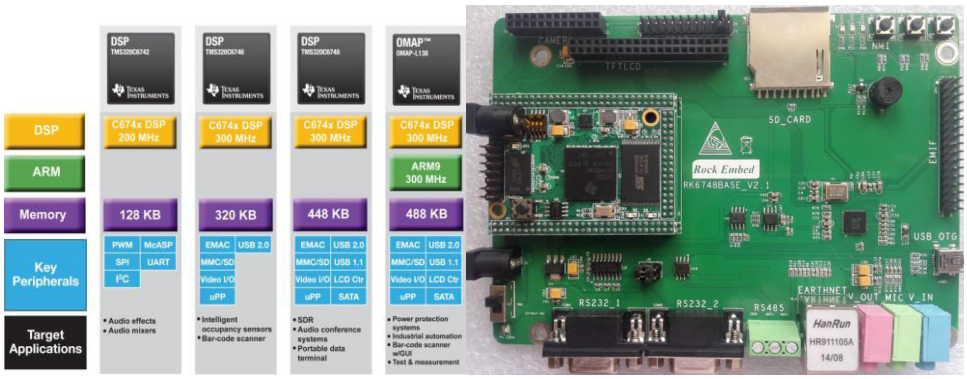

Figure 1 Digital Design and DSP Board

The above design is implemented in windows DSK model and each component is assembled. The software design is set in windows DSK application. The input coordinates are varies for comparing results. Code composer studio is enabled and integrated with DSP board. In this case CCS codes and applied using object file format and load into the hardware. Here, we demonstrate two characteristics

1. Sampling and effect are determined using frequency rate
2. Change the quantizer and memory values using bit allocation method in each per sample

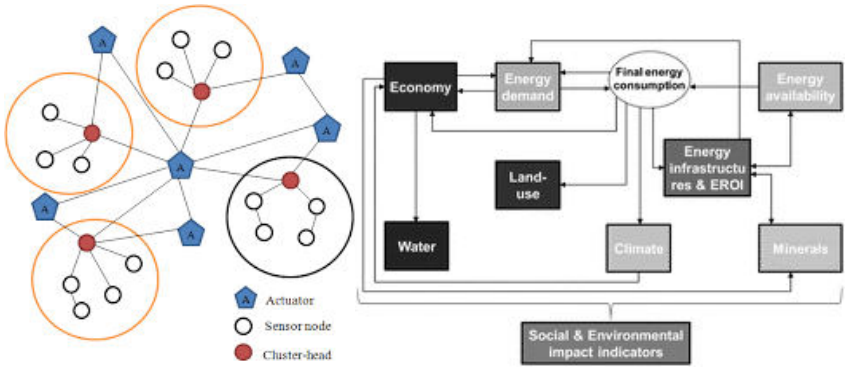

Figure 2 Input from various cluster and senor nodes

The above figure 2 shows that cluster node and sensor values in different real time applications. Consider the network topology structure G is represented as vertex (V), edges (E) and number of entries (W). i and j are node distance. By applying laplacian coordinate, D is a diagonal degree in each entries (W) and L =(1 – (D-1)/2W) * N

For applying graph function f,

$$f_{max} = (1/N)\sum_{i=0,j=0}^{N-1} L(i,j) * \frac{W(i,j)}{N}$$

and calculate Quantizer rate q

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

$q = (L\text{-}1)^{1/N} + \sum_{i=0,j=0}^{N-1} f(i,j) + W(i,j) - \sum_{i=0,j=0}^{N-1} f(i-1,j-1) + W(i-1,j-1)$

This method L increases means the transmitted messages are increases and set fax. If the value reaches high means total error rate is also reduced. So the quantization error rate on each message can be represented as

$q_m = |1/N| \left(\sum_{i=0}^{N-1} qi + (L(i) * W(i))\right)$

Our idea is to minimize the total quantization error in each budget design. So the qm values is tested in each iteration. It can be set as follows,

q_m minimize = |N| and |W| where as L can be calculated and start from i.

Based on this iteration i, the distributed processing algorithms is efficient and produced high propagation results.

IV. IMPLEMENTATION

The above design is implemented in windows DSK platform and codes are applied using Code composer. The below figure show that windows DSK model with our design,

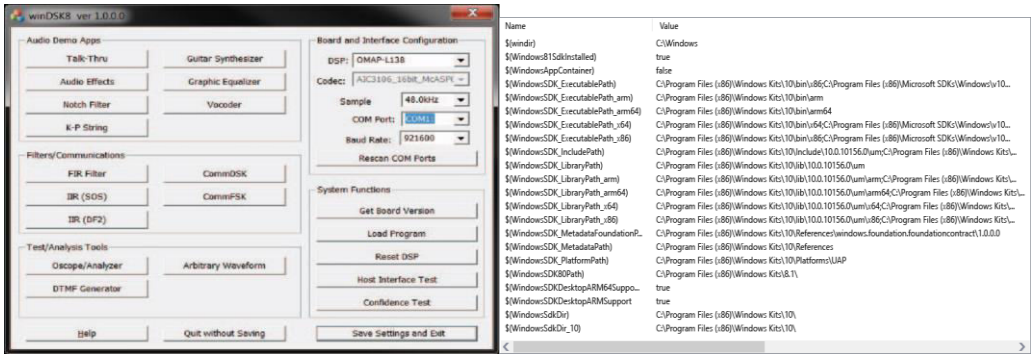

Figure 3 WinDSK Code model and Design

The following factors are considered and set in above winDSK, 1. Analyse the periodic signals, 2. Apply dual tone multi frequency signalling for finding signal to noise ratio, 3. Find impulse and practical implication in each stage, 4. Apply filtering method to find and remove noises, 5. Check various effect and quantizer rate.

The performance of the quantizer is evaluated with first 50 nodes. Each node values are quantized and uniformly distributed. The random code is generated and applied laplacian functions is calculated. Here the denoise factor is set as low pass values t = 1,2,3,5,10,15 and apply chebyshev polynomial approximation with K. The uniform distribution function is applied in each messages and number of bits is represented by N. Optimized quantization method is applied and compare the results.

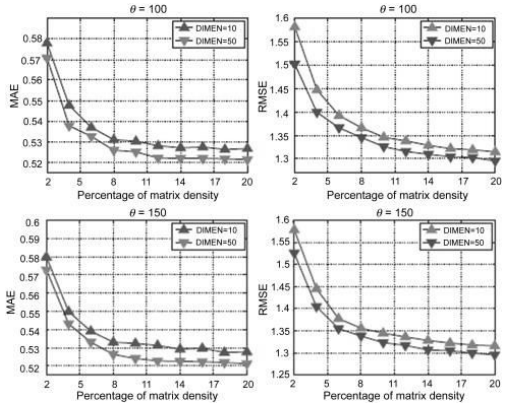

Figure 4 Graph for Quantizer factor 100 and matrix density with number of bits N = 50

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

The above graph shows that after applying optimal bit allocation method provides good result and increase the filter rate without affecting hardware design. The optimized quantization method provides uniform distribution results and performance are notified in above graph. The method is applied to increase the filler values, edges and entries without changing the hardware components.

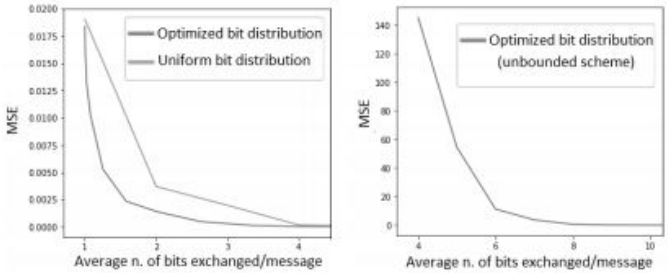

Figure 5 Optimized bit distribution factor results with/without uniform distribution

Finally, we evaluate the efficiency using with and without uniform distribution. Here the bounding scheme is proposed and compare the results. We test the result by varying number bits and different time intervals. Based on above results our proposed method gives good efficiency with low budget design.

V. CONCLUSION

Digital signal processor, dedicated hardware, general purpose components are used in real time applications. We implemented low budget design DSP hardware for handling data and exposing results. We designed model with optimized quantization algorithm and bit allocation scheme. The windows DSK programming kit is used for designing and implementation. This tool is adopting changes and reconfigurable platform. So we changed the nodes and entries values with affecting our design. The performances are compared with uniform and non-uniform distribution factor. Also we changed quantization factor and results are compared. In future, the same design change quantizer factor and increases the nodes.

VI. REFERENCES

1) Isabela Cunha Maia Nobre and Pascal Frossard, “Optimized Quantization In Distributed Graph Signal Processing”, 978-1-5386-4658-8/18/$31.00 ©2019 IEEE
2) Cameron H. G. Wright WY Thad B. Welch Michael G. Morrow , “Reinforcing Signal Processing Theory Using Real-Time Hardware”, 978-1-5090-4117-6/17/$31.00 ©2017 IEEE
3) C. H. G. Wright, T. B. Welch, D. M. Etter, and M. G. Morrow, “Teaching DSP: Bridging the gap from theory to real-time hardware,” ASEE Comput. Educ. J., pp. 14– 26, July–September 2003.
4) M. G. Morrow, C. H. G. Wright, and T. B. Welch, “winDSK8: A user interface for the OMAP-L138 DSP board,” in Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, pp. 2884–2887, May 2011.
5) Xuesong Shi, Hui Feng, Muyuan Zhai, Tao Yang, and Bo Hu, “Infinite impulse response graph filters in wireless sensor networks,” IEEE Signal Processing Letters, vol. 22, no. 8, pp. 1113–1117, 2015.
6) Jiani Liu, Elvin Isufi, and Geert Leus, “Filter design for autoregressive moving average graph filters,” arXiv preprint arXiv:1711.09086, 2017
7) Shengyu Zhu and Biao Chen, “Quantized consensus by the admm: probabilistic versus deterministic quantizers,” IEEE Transactions on Signal Processing, vol. 64, no. 7, pp. 1700–1713, 2016.
8) Shengyu Zhu, Mingyi Hong, and Biao Chen, “Quantized consensus admm for multi-agent distributed optimization,” in Procedings of IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), 2016, pp. 4134–4138.
9) D. I. Shuman, P. Vandergheynst, D. Kressner, and P. Frossard, “Distributed signal processing via chebyshev polynomial approximation,” IEEE Transactions on Signal and Information Processing over Networks, vol. 4, no. 4, pp. 736–751, Dec 2018.
10) S. Manikandan, K. Manikanda Kumaran, "Performance Analysis of Mobile Ad-Hoc Network Routing Protocols using Network Simulator – 2", COMPUSOFT, An International Journal of Advanced Computer Technology, ISSN:2320-0790, Vol.03, Issue: 06, pp-957-960, June-2014
11) Dorina Thanou, Effrosyni Kokiopoulou, Ye Pu, and Pascal Frossard, “Distributed average consensus with quantization refinement,” IEEE Transactions on Signal Processing, vol. 61, no. 1, pp. 194–205, 2013.
12) S. Manikandan, K. Raju, R. Lavanya, R.Hemavathi, "Energy Efficiency Controls on Minimizing Cost with Response Time and Guarantee Using EGC Algorithm",International Journal of Information Technology Insights & Transformations, Vol. 3, No. 1, 2017.
13) D. Thanou and P. Frossard, “Distributed signal processing with graph spectral dictionaries,” in Procedings of the Annual Allerton Conference on Communication, Control, and Computing (Allerton), 2015, pp. 1391–1398.